Amendments to the Specification:

Just before paragraph 0017, please amend the specification as follows:

~~Detailed Description~~ SUMMARY OF THE INVENTION

[0017] Delete

Just before paragraph 0022, please insert the following:

Detailed Description

[0022] Delete

[0028] [[**3.**]] **Example Problems**

[0032] ~~CLE_LINK1~~Waveform 260 represents the D-input if the load offered by NAND gate 120 on path 112 is substantially overestimated. In comparison to waveform 250, waveform 260 occurs sooner in time. Assuming that time duration 267 between clock edge 215 and falling edge 268 (of waveform 260) is less than the corresponding hold time, flip-flop 160 may not latch the data value on D-input accurately (which is undesirable).

[0035] [[**4.**]] **Characterizing Cell Libraries for Accurate Timing Analysis**

[0047] [[**5**.]] **Determining Capacitance Values**

[0053] [[**6.**]] **Software Implementation**

[0061] [[**7**.]] **Conclusion**